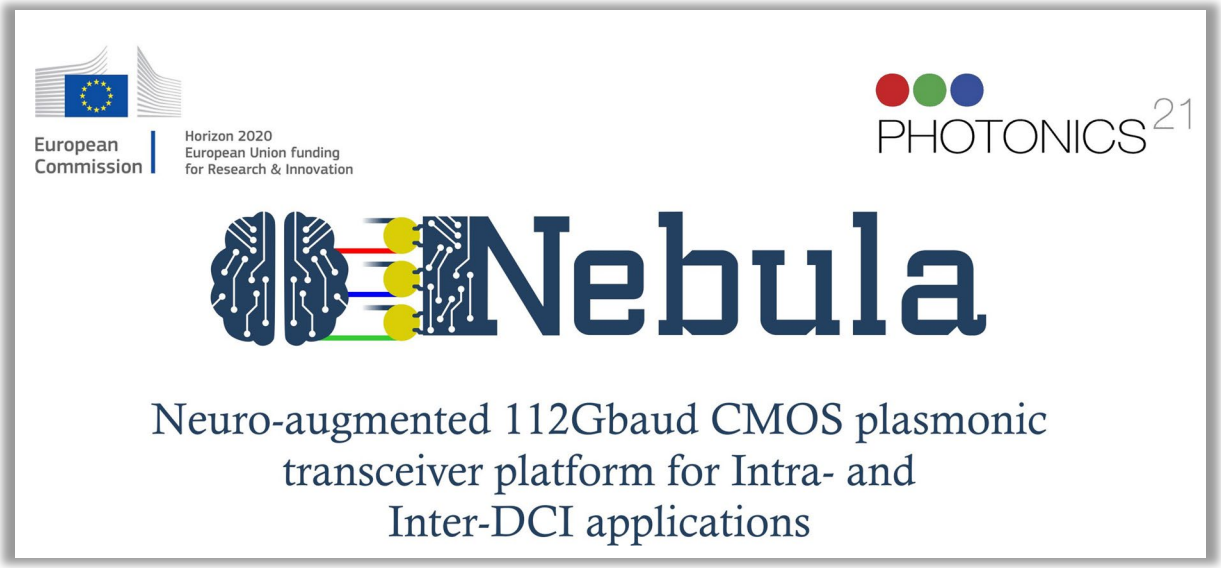

NEBULA factsheet

Grant Agreement:
871658

Duration:
Jan 2020 – Dec 2022 (36 Months)

Coordinator:
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Project website:
URL: www.nebula-h2020.eu

Total budget:
€ 5,999,191.25

Consortium:
Aristotle University of Thessaloniki (GR)
Swiss Federal Institute of Technology in Zurich (CH)
Centre National de la Recherche Scientifique (FR)
Politecnico di Milano (IT)
Interuniversitair Micro-Elektronica Centrum-IMEC (BE)
Institute of Communication and Computer Systems (GR)
Universiteit Gent (BE)
IBM Research GmbH (CH)
Ligentec SA (CH)
III-V Lab (FR)
Mellanox Technologies Ltd (IL)
ADVA Optical Networking SE (DE)

THE CHALLENGE

Data Centers (DC) have turned into the beating heart of today's digital industry, with intra-DC traffic expected to reach 21TB by 2021 increasing by >3x within only five years. An in-depth view to the traffic profiles reveals that East-West traffic exchange is not anymore constrained within a single DC facility, with hyperscale DCs being currently expanded along a distributed DC model comprised of smaller DCs. This new trend will gradually turn the inter-DC and intra-DC interconnect segments to more balanced utilization factors, without however, implying a more relaxed operational framework for the intra-DCI domain: to cope with the rapidly growing traffic demands, switches have increased their capacity faster than Moore's law, rising from 3.2Tbps to the next-generation 25.6Tbps capacity modules within 5 years. Thus, the new DC-roadmap seeks eagerly for a new CMOS-compatible photonic platform offering high bandwidth, low footprint and low power consumption towards the next transceivers' generation as well as the co-package of ASIC switches with optics.

MISSION STATEMENT

This is where NEBULA steps in, aiming to turn the SiN platform in a low-cost, robust and high-speed versatile transceiver platform equipped with

CMOS-compatible plasmonic modulators, thermal stabilizer systems, high-speed PDs and a neuro-augmented DSP realized entirely in the optical domain. NEBULA targets the deployment of a sub-Volt 8-channel 112Gbaud PAM4 O-band transmitter co-packaged with a data generating ASIC, offering a 1.6Tbps aggregate capacity with up to 37% energy savings in Intra-DCI applications. Regarding the Inter-DC links, NEBULA will deploy an 8-channel 112Gbaud 16QAM C-band transceiver prototype, offering an aggregate capacity of 3.2Tbps and requiring just 2.65W per single 400Gbps wavelength, providing in this way an energy efficiency of only 6.625pJ/bit with energy savings of 93%.

PROJECT OBJECTIVES

The overall objective of NEBULA is to develop all the necessary technology building blocks towards low-cost and high-bandwidth transceivers to meet the ever-increasing demands of tomorrow's intra- and inter-DC links. Specifically, the core objectives of NEBULA are to:

- **Turn low loss SiN into a low cost, high-speed versatile transceiver and processing platform for inter- and intra-DCI applications by equipping the platform with:**
  - **two-layer SiN waveguide technology**
  - **Plasmonic slot modulators**
  - **Uni-Travelling Carrier PDs**
- **Demonstrate CMOS plasmonic Resonance Enhanced Modulators (REMs) and IQ modulators on SiN for 112Gbaud intra-and inter-DC interconnects**
- **Develop a mechanism for thermal stabilization (Plasmonic Thermal Stabilizer-PTS) of plasmonic REMs**
- **Deploy an optical 112Gbaud Coherent Receiver assisted by Optical Reservoir Neuromorphic Processing (NP) for DSP free operation**
- **Deploy low cost 112Gbaud PAM4 electronics for energy efficient transceivers**
- **Deploy 8-channel arrays of O-band and C-band modulators with flip-chip compatible optical I/O coupler**
- **Deploy a C-band SiP 8x112Gbaud-16 QAM (3.2Tb/s) transceiver for inter-DC interconnects**
- **Co-package of ASIC and 1.6Tbps O-band driverless transmitter for next Generation 50Tb/s switches**
- **Validate NEBULA transceiver technology in real world intra- and inter-DCI applications**

TECHNOLOGY BREAKTHROUGHS

Plasmonic thermal stabilizer: Thermal stability issues and high temperature variations of co-packaged ASICs and datacom modules are among the most significant challenges that the emerging co-packaged systems need to address. To this end, NEBULA aims to develop a non-invasive thermal stabilization circuitry that will reliably handle temperature variations and thermal drifts of the Plasmonic transmitter modules, targeting to release co-packaged solutions for these harsh temperature environments.

Plasmonic micro-disk modulator: The proposed modulator will feature the most ambitious key metrics of only $5um^2$ footprint, insertion loss of 3dB and power efficiency of less than 50fJ/bit. Capable of operating up to 56Gbaud with PAM4 modulated signals by a driverless single-ended $0.7V_{pp}$ RF signal, this new modulator layout paves the way for lightweight switch engines featuring ASICs co-packaged with Plasmonic-Photonic structures without the use of any extra driving circuit.

Neuro-augmented all-optical DSP: NEBULA will showcase the first DSP-free Rx for coherent demodulation of 16QAM signals up to 112Gbaud. The Neuromorphic Augmented Reservoir Circuit (NARC) will be combined with Uni-Travelling Carrier Photodiodes co-integrated with Semiconductor Optical Amplifiers for enhanced non-linear-reservoir processing. Combing ferroelectric BTO plus HfO_2 memristor elements with a 4:1 EIC Analogue Weighted multiplexer combiner, NEBULA will realize a powerful optoelectronic weighting system, aiming to release once and for all the optical receivers from any DSPs activities.